Government College of Engineering, Karad

(An autonomous Institute of Government of Maharashtra)

One Week FDP

On

Recent Trends in VLSI Technology and Digital ASIC design using CMOS EDA Tool

11th Nov to 16th Nov, 2019

Sponsored by TEQIP Phase III

REGISTRATION FORM

Name: _____

Designation: _____

Institute/Organization: _____

Address for communication: _____

_____

Mobile/Tel: _____

E-mail: _____

Educational Qualification: _____

Experience: _____

Registration Fee: Rs. _____

Payment DU No.: _____

Signature of Applicant

Signature of Head of the Institute (with seal and date)

Patrons

Dr. A.E. Wagh
Director, Technical Education, M.S.
Prof. (Dr.) P. M. Khodke
CPA, NPIU, TEQIP-III, New Delhi
Prof. D. R. Nandanwar
J. D., Regional Office, Pune
Prof. Dr. S. P. Yavalkar
Co-ordinator,SPIU,TEQIP-III,Mumbai,M.S.
Prof. (Dr.) A. T. Pise
Principal, Govt. College of Engineering, Karad
Prof. (Dr.) S. P. Pande
Director,Rajkiya Engineering College,Azamgarh

Conveners

Dr. Ashok M. Sapkal
Head , (ENTC.Dept.),GCEK

Coordinators

Dr. Suhas P. Deshmukh
Associate Professor
suhas.deshmukh@gmail.com

Dr. Deepali S. Shinde (Asst. Professor)
dskshipra@gmail.com
+91 8766548436

Organizing Committee

Amruta U. Mohite **Snehal V. Kumbhar**
Sandip S. Bhandare

Government College of Engineering, Karad

(An Autonomous Institute of Govt. of Maharashtra)

Faculty Development Programme(FDP)

On

Recent Trends in VLSI Technology and Digital ASIC design using CMOS EDA Tool

Sponsored by

Technical Education Quality Improvement Programme

(TEQIP Phase III)

11th Nov to 16 th Nov, 2019

Organized by

Department of

Electronics & Telecommunication Engineering
Government College of Engineering,
Karad – 415124 (M.S.) INDIA
With
Department of Information Technology
Rajkiya Engineering College
Aikbalpur, Sikrapura, Deogaon, Azamgarh
(UP) 276201 India

Website: www.gcekarad.ac.in

Contact Person:
Dr.Deepali S.Shinde
+91 8766548436
Email: fdp.entc.2019@gmail.com

ABOUT INSTITUTE

Govt. College of Engineering Karad is a premier institute in Western Maharashtra established in 1960 due to the efforts of Late Shri. Yashavantrao Chavan. The College is affiliated to Shivaji University, Kolhapur and is acting as a vital education center for many years. Recently the institute also got autonomous status. The institute offers 5 UG programs in Civil, Mechanical, Electrical, Information Technology and Electronics & Telecommunication Engineering and also 6 PG programs in Civil (Construction Management & Structural Engg.), Mechanical (Heat Engg. & Production Engg.), Electrical Engineering (Power Systems) and Master of Computer Applications (MCA).

Amongst the eleven institutes from Maharashtra state selected for participation in the third phase of Technical Education Quality Improvement Program (TEQIP-III) – an ambitious project of Government of India. Govt. College of Engineering, Karad is one of them. The institute is spread over 40 acres of serene and green campus and is a predominantly a residential campus. Karad city is situated on the confluence of rivers Krishna and Koyna and is well connected

ABOUT FDP

As part of TEQIP-III, a Faculty Development Programme (FDP) on "Recent Trends in VLSI Technology and Digital ASIC design using CMOS EDA Tool" is being conducted at GCEK, Maharashtra to the faculty members of Engineering, Research Scholars and other allied disciplines from India. This FDP is devoted to fundamental theory, recent developments and research outcomes addressing the related theoretical and practical aspects of VLSI Technology for engineering applications in wide area. The FDP also aims hands-on using VLSI tools for techniques to be used for implementing applications in VLSI design.

Course objectives

>Gain practical approach to provide solutions to real time problems by designing industry grade models in VLSI domain

>Implement real time problems using VLSI design

>Verify the functionality of design model by high end verification tool like CMOS EDA.

> Research scope in VLSI with demonstration on VLSI kits with advanced training material will be provided

Program Outcome

The participant should be able to understand and apply different soft computing techniques and machine learning algorithms to the various engineering applications.

COURSE INSTRUCTOR

Faculties from reputed institutes like IITs/NITs, Universities and Industries.

ELIGIBILITY

Faculty members and research scholars from AICTE approved Engineering and polytechnic Institutes and Industrial persons are eligible to participate. Participants are required to register in advance using the enclosed form.

COURSE CONTENTS

- Exposure to VLSI/ ASIC Design
- Hands on VLSI Backend and Frontend design tool
- To study CMOS VLSI design issues
- Transistor sizing W/L calculations, Lambda parameters
- Combinational and Sequential CMOS design
- Design rule check with technology scaling
- Power I/O and clock design

REGISTRATION

The Participants who will receive confirmation mail will have to send the filled and duly signed registration form along with the copy of registration fees payment proof by email

REGISTRATION FEES

Student Participant: Rs. 1000/- each
Faculty Participant: Rs. 2000/- each
Industry Participant: Rs. 4000/-each

The registration fees shall be paid on-line after receipt of acceptance from us. Traveling, Lodging, boarding and other expenses will have to be borne by the participant. Accommodation will have to be managed by the participants only. However, the guidance will be provided for accommodation.

The link for online payment is:

https://www.onlinesbi.com/sbicollect/icollecthome.htm

Note: For any queries regarding payment, please contact the coordinators.

1. **Registration fee is inclusive of breakfast, high tea, working lunch and program kit**
2. **Accommodation on first come first serve basis**

DATE AND VENUE

The FDP will be held 11th Nov to 16th Nov, 2019 at VLSI lab, ENTC Department Govt. College of Engg., Karad

- **Last Date of Registration: 31st Oct 2019.**
- **Notification of acceptance by e-mail: 5th Nov 2019.**
- **Scanned copy of Completed Registration form should be send by email to course Co-coordinators.**